UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,908	12/17/2003	Frederic Josso	003921.00137	4026

22907 7590 04/12/2007		EXAMINER
BANNER & WITCOFF, LTD. 1100 13th STREET, N.W. SUITE 1200 WASHINGTON, DC 20005-4051		WHITMORE, STACY
	ART UNIT	PAPER NUMBER
	2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

	Application No.	Applicant(s)
Office Action Summary	10/736,908	JOSSO ET AL.
	Examiner	Art Unit
	Stacy A. Whitmore	2825

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status   3/26/07

1) ☒ Responsive to communication(s) filed on ~~3/27/3007~~.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-33* is/are pending in the application.

    4a) Of the above claim(s) *22-33* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-21* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *17 December 2003* is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date *3/8/05*.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.   Applicant's election without traverse of claims 1-21 in the reply filed on March 27, 2007 is acknowledged.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-6, 9-11, and 13-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Butts, M. (European Patent 0 651 343 A1).

3.   Butts was cited on the IDS dated March 8, 2005.

4.   As for the claims, Butts discloses the invention as claimed, including:

1. An emulation logic board, comprising: at least one integrated circuit having reconfigurable logic resources [fig. 1, realizer hardware system; abstract; pg. 2, pg. 7, pg. 8]; and on-board processing resources, in communication with the at least one integrated circuit, operable to configure the integrated circuit [fig. 1, realizer hardware system; abstract; pg. 2, pg. 7, pg. 8];

2. The emulation logic board of claim 1, further comprising a plurality of integrated circuits, each having reconfigurable logic resources, the on-board processing resources being operable to configure each of the reconfigurable logic resources of each of the integrated circuits [fig. 1, realizer hardware system; abstract; pg. 2, pg. 7, pg. 8];

3. The emulation logic board of claim 1, wherein the integrated circuit further includes reconfigurable input/output resources, the on-board processing resources being further

operable to configure the reconfigurable input/output resources [fig. 1, realizer hardware system; abstract; pg. 2, pg. 7, pg. 8, especially pg. 7];

4. The emulation logic board of claim 1, wherein the on-board processing resources comprise:

memory having stored therein programming instructions for configuring the integrated circuit; and a processor coupled to the memory to execute the programming instructions [fig. 1, realizer hardware system; abstract; pg. 2, pg. 7, pg. 8, especially fig. 1, host interface and config system];

5. The emulation logic board of claim 1, further comprising reconfigurable interconnects in communication with the integrated circuit and the on-board processing resources, wherein the on-board processing resources are operative to configure the reconfigurable interconnects [pgs. 8-11];

6. The emulation logic board of claim 1, wherein the on-board processing resources are operable to configure the integrated circuit in response to external commands [pg. 8, lines 42-50];

9. The emulation logic board of claim 1, wherein the integrated circuit comprises on-chip data processing resources operative to assist the on-board processing resources to perform the configuration of the integrated circuit [pg. 8, lines 42-50];

10. The emulation logic board of claim 1, wherein the on-board processing resources are further operable to perform emulation functions on a configured integrated circuit [pg. 8, lines 42-50, pg. 2, lines 25-27];

11. The emulation logic board of claim 10, wherein the emulation functions comprise generating testing stimuli and applying testing stimuli to an appropriate pin of the at least one integrated circuit [pg. 2, lines 30-31, operating the device discloses that the device is being tested as if it were operating to emulate the design functions; pg. 3, lines 5-9];

13. The emulation logic board of claim 10 wherein the on-board processing resources are operable to perform emulation functions responsive to external commands [fig. 1, host to realizer system, pg. 3, lines 14];

14. In an emulation logic board comprising at least one integrated circuit, having reconfigurable logic resources and on-board processing resources, in communication with the at least one integrated circuit, a method of configuring the emulation logic board comprising:

receiving, by the on-board processing resources, a command for configuring the logic board; and configuring the emulation logic board in accordance with the command received by the on-board processing resources [fig. 1, realizer hardware system; abstract; pg. 2, pg. 7, pg. 8];

15. The method of claim 14, wherein configuring the emulation logic board in accordance with the external command comprises: locally generating on the emulation logic board, by the on-board processing resources, a configuration signal to configure the at least one integrated circuit; and applying the locally generated configuration signal to the integrated circuit [pg. 2, lines 25-27, pg. 8, lines 42-45];

16. The method of claim 14, wherein the emulation logic board further includes reconfigurable interconnects in communication with the integrated circuit and the on-board processing resources, and the on-board resources are operative to configure the reconfigurable interconnects [pgs. 2, 7-10, and especially pg. 2, lines 25-27, pg. 8, lines 42-45], and wherein configuring the emulation board in accordance with the command comprises:

locally generating on the emulation logic board, by the on-board processing resources, a configuration signal to configure the at least one of the reconfigurable interconnects; and applying the locally generated configuration signal to the at least one reconfigurable interconnect [pgs. 2, 7-10, and especially pg. 2, lines 25-27, pg. 8, lines 42-45];

17. The method of claim 14, wherein the integrated circuit further comprises on-chip processing resources, configuring the integrated circuit is at least partially performed in conjunction with on-chip data processing resources [pgs. 2, 7-10, and especially pg. 2, lines 25-27, pg. 8, lines 42-45];

18. An emulation system comprising: a workstation having electronic design automation (EDA) software to partition an integrated circuit (IC) design into a plurality of partitions;

and at least one emulation logic board in communication with the workstation,
comprising:

at least one integrated circuit having reconfigurable logic resources, and on-board
processing resources, in communication with the at least one integrated circuit and
operable to configure the integrated circuit in response to commands from the EDA
software of the workstation [fig. 1, realizer hardware system; abstract; pg. 2, pg. 3, lines
10-14, pg. 7, pg. 8];

19. The emulation system of claim 18, comprising a plurality of emulation logic boards
[pg. 2, lines 52-54];

20. The emulation system of claim 18 wherein the emulation logic board further
comprises reconfigurable interconnects in communication with the integrated circuit and
the on-board processing resources, wherein the on-board resources are operative to
configure the reconfigurable interconnects [pgs. 2, 7-10, and especially pg. 2, lines 25-
27, pg. 8, lines 42-45];

21. The emulation system as set forth in claim 18, wherein the on-board processing
resources are further operable to perform emulation functions on a configured
integrated circuit in response to commands from the EDA software of the workstation
[pgs. 2, 7-10, and especially pg. 2, lines 25-27, pg. 8, lines 42-45, pg. 3, lines 10-14].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed
> or described as set forth in section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are such that the subject
> matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was
> made.

5.   Claims 7-8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butts, M. (European Patent 0 651 343 A1) in view of Tseng (US Patent Application Publication 2002/0049578).

6.   As for the claims, Butts discloses the invention substantially as claimed, including the emulation logic system and method as cited above in the rejections of claims 1-6, 9-11, and 13-21.

Butts does not specifically disclose

7. The emulation logic board of claim 6, wherein the external commands comprise a data packet.

8. The emulation logic board of claim 7, wherein the data packet comprises: a packet header; a command field following the packet header; a parameter field following the command field; and an end-of-packet marker following the parameter field [];

12. The emulation logic board of claim 10, where the emulation functions comprise: locally determining emulation state elements of a design being emulated; reading state data of the emulation state elements to detect occurrence of certain events; and reporting the occurrence of the events upon detection [];

Tseng discloses

7. The emulation logic board of claim 6, wherein the external commands comprise a data packet [abstract, paragraph 0019];

8. The emulation logic board of claim 7, wherein the data packet comprises: a packet header; a command field following the packet header; a parameter field following the command field; and an end-of-packet marker following the parameter field [abstract, paragraph 0019, figs. 1,3,6, 11a-11d, and 16];

12. The emulation logic board of claim 10, where the emulation functions comprise: locally determining emulation state elements of a design being emulated; reading state data of the emulation state elements to detect occurrence of certain events; and reporting the occurrence of the events upon detection [fig. 9, paragraphs 0075-0076].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Butts and Tseng because using Tseng's system which utilizes data packets, and state conditions of the elements would have optimized communications between the host and the hardware emulator (see Tseng, paragraph 0010).

7.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
March 30, 2007